REMARKS

The Applicants thank the Examiner for the careful examination of this application and respectfully request the entry of the amendments indicated hereinabove.

Claims 3 and 8-11 are pending and rejected. Claims 3, 9, and 11 are amended and Claim 8 is canceled hereinabove.

In response to the objection to the Specification, the Applicants have amended the Abstract Of The Disclosure in accordance with the Examiner's suggestions. The Applicants respectfully traverse the Examiner's requirement to enclose the numerical references in parentheses. Such extra effort is not required by 37 CFR 1.72. In addition, contrary to the Examiners' statement on page 2, MPEP 608.01(b) does not require this amendment to the Abstract. In fact, none of the "Sample Abstracts" contained in MPEP 608.01(b) (page 600-67) contain numerical references in parentheses.

In response to the objection to the Claims, the Applicants have amended Claim 3 and canceled Claim 8 hereinabove. The Applicants respectfully traverse the Examiner's restriction requirement that precipitated this divisional and therefore these claim changes. The Applicants reassert their election with traverse because, as the Applicants stated previously, "no reason exists for concluding that each Species has attained recognition in the art as a separate status or field of search." The Applicants submit that their position is supported by the fact that both

divisionals were prosecuted by the same Examiner as the parent case, both divisionals are being prosecuted in the same art unit, and both divisionals have pending Office Actions that are virtually identical to the pending Office Action in the parent case (the majority of the pending parent Office Action appears unchanged in the pending Office Actions of the two divisionals). Therefore, the Applicants fail to understand the justification for being forced to pay three application fees to have all of the inventions in the full claim set of the initial patent application prosecuted by the USPTO.

Amended Claim 3 positively recites that the cap layer of the PMOS transistor is coupled to a majority of the top surface of the lightly doped drain but the cap layer is separated from the gate oxide. Amended Claim 3 also positively recites that the cap layer is comprised of a high dielectric constant material. These advantageously claimed features are not taught or suggested by the Tsuchiya et al. article, or the patents granted to Yu et al., or Xiang et al.; either alone or in combination.

Tsuchiya et al. teaches the use of a thin offset spacer (Fig. 1 and last two lines of column 1 of page 1), not the cap layer as advantageously claimed. The advantageously claimed cap layer (element 9 of the Applicant's Figure) runs the majority of the length of the LDD implant (element 12 of the Applicant's Figure). Conversely, the offset spacer taught by Tsuchiya et al. (Fig. 1) is a thin spacer that protects the channel under the gate but not the LDD implant. Moreover, Tsuchiya et al. teaches that the majority of the offset spacer is comprised of SiO_2 (last two lines of column 1 of page 1), not a high-k material as advantageously claimed.

Yu et al. teaches a gate dielectric made of high-k material (column 3 lines 15-16). The Applicants submit that teachings concerning the structure of the gate stack are irrelevant to the Applicants' advantageously claimed spacer region structure. Furthermore, the Applicants submit that Yu et al. teaches away from the advantageously claimed spacer structure because Yu et al. teaches the use of a spacer structure containing no high-k materials (column 4 lines 7 and 21-26).

Xiang et al. teaches a transistor structure that has a liner coupled to the gate oxide (FIGS. 1, 3B and 3C; column 5 lines 50-54). Therefore, Xiang et al. does not teach or suggest a cap layer separated from the gate oxide, as advantageously claimed.

Therefore, the Applicants respectfully traverse the Examiner's rejection of Claim 3 and respectfully assert that Claim 3 is patentable over the Tsuchiya et al. article, and the patents granted to Yu et al., and Xiang et al.; either alone or in combination.

Amended Claim 9 positively recites that the cap layer of the PMOS transistor is coupled to a majority of the top surface of the lightly doped drain but the cap layer is separated from the gate oxide. Amended Claim 9 also positively recites that the cap layer is comprised of a high dielectric constant material. These advantageously claimed features are not taught or suggested by the Tsuchiya et al. article, or the patents granted to Yu et al. ('214), Xiang et al. or Yu et al. ('307); either alone or in combination.

Tsuchiya et al. teaches the use of a thin offset spacer (Fig. 1 and last two lines of column 1 of page 1), not the cap layer as advantageously claimed. The advantageously claimed cap layer (element 9 of the Applicant's Figure) runs the majority of the length of the LDD implant (element 12 of the Applicant's Figure). Conversely, the offset spacer taught by Tsuchiya et al. (Fig. 1) is a thin spacer that protects the channel under the gate but not the LDD implant. Moreover, Tsuchiya et al. teaches that the majority of the offset spacer is comprised of SiO_2 (last two lines of column 1 of page 1), not a high-k material as advantageously claimed.

Yu et al. ('214) teaches a gate dielectric made of high-k material (column 3 lines 15-16). The Applicants submit that teachings concerning the structure of the gate stack are irrelevant to the Applicants' advantageously claimed spacer region structure. Furthermore, the Applicants submit that Yu et al. ('214) teaches away from the advantageously claimed spacer structure because Yu et al. ('214) teaches the use of a spacer structure containing no high-k materials (column 4 lines 7 and 21-26).

Xiang et al. teaches a transistor structure that has a liner coupled to the gate oxide (FIGS. 1, 3B and 3C; column 5 lines 50-54). Therefore, Xiang et al. does not teach or suggest a cap layer separated from the gate oxide, as advantageously claimed.

Yu et al. ('307) teaches the use of high-k materials as gate dielectrics (column 4 lines 6-7 and 55-56). Furthermore, Yu et al. ('307) teaches the use of

sidewall spacers made from standard-k materials (column 7 lines 1-4, column 10 lines 1-2). Therefore, Yu et al. ('307) teaches away from the advantageously claimed cap layer. Moreover, Yu et al. ('307) teaches away from being combined in the manner asserted in the Office Action because 1. Yu et al. ('307) specifies that the spacer material is not high-k material (column 7 lines 1-4, column 10 lines 1-2) and 2. if Tsuchiya et al. and Yu et al. ('307) were combined (in opposition to the teachings of Yu) then the resulting structure would be a high-k offset spacer that does not cover the LDD in the manner of the advantageously claimed cap layer.

Therefore, the Applicants respectfully traverse the Examiner's rejection of Claim 9 and respectfully assert that Claim 9 is patentable over the Tsuchiya et al. article, and the patents granted to Yu et al. ('214), Xiang et al. and Yu et al. ('307); either alone or in combination. Furthermore, Claim 10 is allowable for depending on allowable independent Claim 9 and, in combination, including limitations not taught or described in the references of record.

Amended Claim 11 positively recites that the cap layer of the PMOS transistor is coupled to a majority of the top surface of the lightly doped drain but the cap layer is separated from the gate oxide. Amended Claim 11 also positively recites that the cap layer is comprised of hafnium silicon oxynitride. These advantageously claimed features are not taught or suggested by the Tsuchiya et al. article, or the patents granted to Yu et al. ('214), Xiang et al. or Yu et al. ('307); either alone or in combination.

Tsuchiya et al. teaches the use of a thin offset spacer (Fig. 1 and last two lines of column 1 of page 1), not the cap layer as advantageously claimed. The advantageously claimed cap layer (element 9 of the Applicant's Figure) runs the majority of the length of the LDD implant (element 12 of the Applicant's Figure). Conversely, the offset spacer taught by Tsuchiya et al. (Fig. 1) is a thin spacer that protects the channel under the gate but not the LDD implant. Moreover, Tsuchiya et al. teaches that the majority of the offset spacer is comprised of SiO_2 (last two lines of column 1 of page 1), not a high-k material as advantageously claimed.

Yu et al. ('214) teaches a gate dielectric made of high-k material (column 3 lines 15-16). The Applicants submit that teachings concerning the structure of the gate stack are irrelevant to the Applicants' advantageously claimed spacer region structure. Furthermore, the Applicants submit that Yu et al. ('214) teaches away from the advantageously claimed spacer structure because Yu et al. ('214) teaches the use of a spacer structure containing no high-k materials (column 4 lines 7 and 21-26).

Xiang et al. teaches a transistor structure that has a liner coupled to the gate oxide (FIGS. 1, 3B and 3C; column 5 lines 50-54). Therefore, Xiang et al. does not teach or suggest a cap layer separated from the gate oxide, as advantageously claimed.

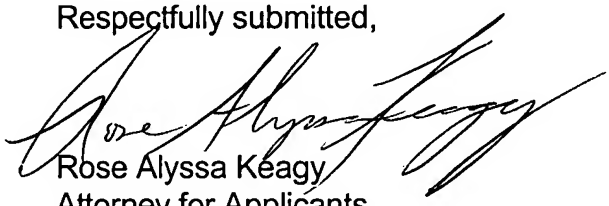
Yu et al. ('307) teaches the use of high-k materials as gate dielectrics (column 4 lines 6-7 and 55-56). Furthermore, Yu et al. ('307) teaches the use of sidewall spacers made from standard-k materials (column 7 lines 1-4, column 10

lines 1-2). Therefore, Yu et al. ('307) teaches away from the advantageously claimed cap layer. Moreover, Yu et al. ('307) teaches away from being combined in the manner asserted in the Office Action because 1. Yu et al. ('307) specifies that the spacer material is not high-k material (column 7 lines 1-4, column 10 lines 1-2) and 2. if Tsuchiya et al. and Yu et al. ('307) were combined (in opposition to the teachings of Yu) then the resulting structure would be a high-k offset spacer that does not cover the LDD in the manner of the advantageously claimed cap layer.

Therefore, the Applicants respectfully traverse the Examiner's rejection of Claim 11 and respectfully assert that Claim 11 is patentable over the Tsuchiya et al. article, and the patents granted to Yu et al. ('214), Xiang et al. and Yu et al. ('307); either alone or in combination.

For the reasons stated above, this application is believed to be in condition for allowance. Reexamination and reconsideration is requested.

Respectfully submitted,



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